REMARKS

Claims 1-10 were pending in the present application. By virtue of this response, claims 1 and 8 have been amended. Accordingly, claims 1-10 are currently under consideration. Amendment and cancellation of certain claims is not to be construed as a dedication to the public of any of the subject matter of the claims as previously presented. No new matter has been added.

Rejections under 35 U.S.C. § 102(e)

Claims 1-10 are rejected under 35 U.S.C. § 102(e) as allegedly being anticipated by Hamaguchi (U.S. 6,862,213, hereinafter the Hamaguchi reference). Applicants respectfully traverse these rejections.

Applicants submit that Hamaguchi does not teach at least the claim element that "a variable resistor having a resistance value thereof reversibly changed in accordance with a voltage applied thereto." From the cited portion (see Hamaguchi, column 12, lines 29-32, and in column 7, lines 4-7 and lines 56-57), the Hamaguchi reference simply states that the resistance state is variable depending on the applied voltage. In column 5, lines 8-12, it simply discloses that a resistance value is variable according to the application of electrical stress. Nowhere in the Yamaguchi reference teaches or suggests about how to change polarity of the voltages applied to the variable resistor as disclosed in the present application.

In addition, Hamaguchi fails to teach the amended claim element that "the resistance value is increased by application of a voltage having a prescribed polarity to one end of the variable resistor and by application of a voltage having a same polarity as the prescribed polarity to the other end of the variable resistor, and the resistance value is decreased by application of a voltage having a prescribed polarity to one end of the variable resistor and by application of a voltage having an opposite polarity with respect to the prescribed polarity to the other end of the variable resistor." This added claim limitation relates to how data is written to or erased from a memory cell.

For at least the reasons stated above, the present rejections to the independent claims 1 and 8, and their corresponding dependent claims 2-7 and 9-10 should be withdrawn.

Support for Amended Claims 1 & 8

The support for the currently amended claims 1 and 8 are described below. Specifically, "[T]he variable resistor 30 connected to the drain region 23 ... is connected to the respective bit line" (see page 26, lines 1-4), and "... [T]he gate is connected to the word line" (see page 17, lines 7-8). One skilled in the art appreciate that voltages applied to the word line and the bit line at the same time would effectively represent voltages applied to both ends of the variable resistor.

From the specification of the pending application, a voltage of a prescribed polarity is applied to the bit line, and a voltage is applied to the word line, so that data is written to the memory cell controlled by the word line and the bit line (see page 17, lines 10-15). A voltage of a polarity opposite to the prescribed polarity is applied to the bit line, and a voltage applied to the word line, so that data is erased from the one memory cell (see page 17, lines 17-23). In other words, "... the data write operation and the data erase operation are switched by merely inverting the polarity of the voltage applied to the bit line" (see page 27, lines 23-24 to page 28, lines 1-2).

One skilled in the art would be able to interpret these disclosed statements to mean that voltages having the same polarity applied to both ends of the variable resistor would result in data being written, while voltages having opposite polarity applied to both ends of the variable resistor would result in data being erased.

The examples disclosed on pages 26 and 27 further demonstrate this phenomenon. For writing data to the selected memory cell 10, for example, $Vw1 = 3.0$ V is applied to the word line and $Vb1 = 5.0$ V is applied to the bit line. "As a result, the resistance value of the varilable resistor 30 of the selected memory cell 10 is changed from an initial state." (see page 26, lines 21-24 to page 27, lines 1-8) For erasing data from the selected memory cell 10, for example, $Vw1 = 3.0$ V is applied to the word line and $Vb1 = -5.0$ V is applied to the bit line. "As a result, the resistance value

of the variable resistor 30 of the selected memory cell 10 is returned to the initial state." (see page 27, lines 10-21)

Moreover, Figure 7 illustrates the change in the resistance value (i.e., an increase in the resistance value) when a pulse voltage having the same polarity is applied a plurality of times (see Figure 7, and page 24, lines 19-24). Accordingly, the resistance value of the variable resistor is changed (i.e., increased) from the initial state during the data write operation which corresponds to voltages having the same polarity applied to both ends of said resistor. The resistance value is returned to the initial state (i.e., decreased) during the data erase operation which corresponds to voltages having opposite polarity applied to both ends of said resistor.

Therefore, the specification of the pending application teaches how the variable resistor is reversibly changed in accordance with a voltage applied thereto as recited in claims 1-10, and thus support is present in the specification for the amendments to claims 1 and 8.

CONCLUSION

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue. If it is determined that a telephone conference would expedite the prosecution of this application, the Examiner is invited to telephone the undersigned at the number given below.

In the event the U.S. Patent and Trademark office determines that an extension and/or other relief is required, applicant petitions for any required relief including extensions of time and authorizes the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to Deposit Account No. 03-1952 referencing docket no. 299002057400. However, the Commissioner is not authorized to charge the cost of the issue fee to the Deposit Account.

Dated: January 19, 2006

Respectfully submitted,

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